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(71) Applicant: QUALCOMM INCORPORATED [US/US]; 5775 Morehouse Drive, San Diego, CA 92121 (US).

(72) Inventors: AGRAWAL, Avneesh; 655 South Fair Oaks #F109, Sunnyvale, CA 94086 (US). ZOU, Quizhen; 5791 Rutgers Road, La Jolla, CA 92037 (US).

(74) Agents: WADSWORTH, Philip, R. et al.; Qualcomm Incorporated, 5775 Morehouse Drive, San Diego, CA 92121 (US).

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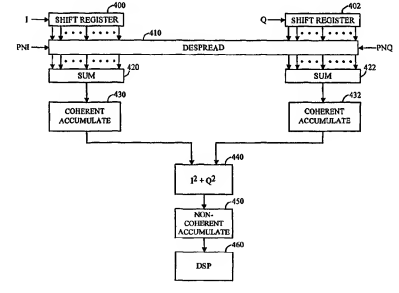

(57) Abstract

A novel and improved method and apparatus for searching is described. Channel data is despread utilizing a matched filter structure. The in-phase and quadrature amplitudes of the despreading (410) delivered to coherent accumulators (430, 432) to sum for a programmable duration of time. The amplitude accumulations are squared and summed (440) to produce an energy measurement. The energy measurement is accumulated for a second programmable time to perform non-coherent accumulation (450). The resulting value is used to determine the likelihood of a pilot signal at that offset. Each matched filter structure comprises an N-value shift register for receiving data, a programmable bank of taps to perform despreading and optional Walsh decovering, and an adder structure to sum the resulting filter tap calculations.

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PROGRAMMABLE MATCHED FILTER SEARCHER

BACKGROUND OF THE INVENTION

I. Field of the Invention

The present invention relates to communications. More particularly, the present invention relates to a novel and improved method and apparatus for detecting a pilot signal with a programmable matched filter searcher.

II. Description of the Related Art

Pseudorandom noise (PN) sequences are commonly used in direct sequence spread spectrum communication systems such as that described in the IS-95 over the air interface standard and its derivatives such as IS-95-A and ANSI J-STD-008 (referred to hereafter collectively as the IS-95 standard) promulgated by the Telecommunication Industry Association (TIA) and used primarily within cellular telecommunications systems. The IS-95 standard incorporates code division multiple access (CDMA) signal modulation techniques to conduct multiple communications simultaneously over the same RF bandwidth. When combined with comprehensive power control, conducting multiple communications over the same bandwidth increases the total number of calls and other communications that can be conducted in a wireless communication system by, among other things, increasing the frequency reuse in comparison to other wireless telecommunication technologies. The use of CDMA techniques in a multiple access communication system is disclosed in U.S. Patent No. 4,901,307, entitled "SPREAD SPECTRUM COMMUNICATION SYSTEM USING SATELLITE OR TERRESTRIAL REPEATERS", and U.S. Patent No. 5,103,459, entitled "SYSTEM AND METHOD FOR GENERATING SIGNAL WAVEFORMS IN A CDMA CELLULAR TELEPHONE SYSTEM", both of which are assigned to the assignee of the present invention and incorporated by reference herein.

FIG. 1 provides a highly simplified illustration of a cellular telephone system configured in accordance with the use of the IS-95 standard. During operation, a set of subscriber units **10a - d** conduct wireless communication by establishing one or more RF interfaces with one or more base stations **12a - d** using CDMA modulated RF signals. Each RF interface between a base station **12** and a subscriber unit **10** is comprised of a forward link signal transmitted

from the base station **12**, and a reverse link signal transmitted from the subscriber unit. Using these RF interfaces, a communication with another user is generally conducted by way of mobile telephone switching office (MTSO) 14 and public switch telephone network (PSTN) **16**. The links between base stations **12**, MTSO **14** and PSTN **16** are usually formed via wire line connections, although the use of additional RF or microwave links is also known.

Each subscriber unit **10** communicates with one or more base stations **12** by utilizing a rake receiver. A RAKE receiver is described in U.S. Patent No. 5,109,390 entitled "DIVERSITY RECEIVER IN A CDMA CELLULAR TELEPHONE SYSTEM", assigned to the assignee of the present invention and incorporated herein by reference. A rake receiver is typically made up of one or more searchers for locating direct and multipath pilot from neighboring base stations, and two or more fingers for receiving and combining information signals from those base stations. Searchers are described in co-pending U.S. Patent Application 08/316,177, entitled "MULTIPATH SEARCH PROCESSOR FOR SPREAD SPECTRUM MULTIPLE ACCESS COMMUNICATION SYSTEMS", filed September 30, 1994, assigned to the assignee of the present invention and incorporated herein by reference.

Inherent in the design of direct sequence spread spectrum communication systems is the requirement that a receiver must align its PN sequences to those of the base station. In IS-95, each base station and subscriber unit uses the exact same PN sequences. A base station distinguishes itself from other base stations by inserting a unique offset in the generation of its PN sequences. In IS-95 systems, all base stations are offset by an integer multiple of 64 chips. A subscriber unit communicates with a base station by assigning at least one finger to that base station. An assigned finger must insert the appropriate offset into its PN sequence in order to communicate with that base station. It is also possible to differentiate base stations by using unique PN sequences for each rather than offsets of the same PN sequence. In this case, fingers would adjust their PN generators to produce the appropriate PN sequence for the base station to which it is assigned.

Subscriber units locate base stations by utilizing searchers. FIG. 2 depicts a common type of serial correlator used for searching in a subscriber unit. This searcher is described in U.S. Patent No. 5,644,591, entitled "METHOD AND APPARATUS FOR PERFORMING SEARCH ACQUISITION IN A CDMA COMMUNICATIONS SYSTEM", issued July 1, 1997, assigned to the assignee of the present invention and incorporated herein by reference.

In FIG. 2, antenna **20** receives a signal comprising pilot signal transmissions from one or more base stations. The signal is downconverted and amplified in receiver **21**, which generates an in-phase (I) and quadrature (Q) component of the received signal and delivers them to despreader **22**. I and Q PN sequence generator **23** produces the proper I and Q PN sequences for a candidate offset as directed by searcher controller **27**. Despreader **22** receives the I and Q PN sequences and despreads the I and Q received signals, passing the results to coherent accumulators **24** and **25**. These accumulators integrate the amplitudes of the despread I and Q signals for a period of time specified by searcher controller **27**. Coherent accumulators **24** and **25** sum the I and Q amplitudes for a period of time in which the phase of the incoming signal is approximately constant. The results are passed to energy calculation block **26** where the I and Q coherent accumulations are squared and summed. The result is accumulated in non-coherent accumulator **28**. Non-coherent accumulator **28** is summing energies, and so the constant phase requirements of coherent accumulation do not apply. Energy is accumulated for a period of time as directed by searcher controller **27**. The result is compared in threshold compare **29**. Once the process is completed for the candidate offset programmed in I and Q PN sequence generator **23**, searcher controller **27** directs a new candidate offset to be analyzed.

The searcher as just described has the advantage of great flexibility. Any number of coherent integrations, C, (within the limits of coherence time) may be performed on a candidate offset, and any number of non-coherent accumulations, M, may be performed. Any number of hypotheses to search, L, can be searched. The overall search time for a window of L hypotheses is then given by L*C*M. The drawback of this architecture is that each candidate is calculated in a serial manner. To reduce search time for given M and N requires that duplicative hardware be added.

FIG. 3 shows an alternative searcher architecture, commonly called a matched filter searcher. For a discussion of this method, see Simon, Omura, Scholtz & Levitt, SPREAD SPECTRUM COMMUNICATIONS HANDBOOK, pp. 815-822, McGraw-Hill, Inc., New York (1994).

An incoming signal is received at antenna **30** and passed to receiver **31** for downconversion and amplification. I and Q channels are then delivered to delay chains **36** and **38**, respectively. Each delay chain contains N delay elements labeled DI1-DIN and DQ1-DQN. The output of each delay element is multiplied by a PN value loaded into tap value chains **35** and **37**. The tap values are created with I and Q PN generators and loaded or hard coded into

multiplication elements labeled PNI1-PNIN and PNQ1-PNQN. Note that in the simple case, the tap values include only 1 and -1, so inverters (or negaters) take the place of actual multipliers. The associations of delay element outputs and tap values is shown in FIG. 3. The tap values are made up of a portion of the PN sequence which is used to correlate with the incoming data. The results of all the multiplications are delivered to adders **34** and **32**, where they are summed. The results are then squared and summed to create an energy calculation in block **33**, the result of which is compared in threshold compare **39**. Whenever the energy result is high, it is likely that a base station pilot exists and its PN generators are aligned with the portion of the PN sequences contained in the tap elements. In a single pass of the time required to cycle through the entire PN sequence, every possible offset has an energy value calculated for it.

The benefits of this architecture include parallel calculations of N hypotheses such that a result is generated once for every cycle that the delay elements are updated. This architecture is optimal for the case where the number of hypotheses to be searched, L, is equal to the entire PN space, the number of coherent accumulations desired, C, is equal to the number of taps, N, and the number of non-coherent accumulations, M, is set to one. In this scenario, the total search time will be L + N (assuming that it requires N cycles to fill the delay elements with valid data). The delay elements may already contain valid data, and in any case N is typically much smaller than the PN space, so the search time is essentially related directly to L. Compare this with the time for the serial correlator searcher described above: L*C*M = L*C.

The maximum value for N is given by the coherence time. The matched filter portion of the searcher is essentially performing coherent accumulation of despread input signals. This is the same constraint for maximum C in the prior architecture. To increase the number of non-coherent accumulations requires adding memory storage to hold an intermediate calculation for every hypothesis to search, or L additional memory elements. The search time then for M>1 is given by M*PN, where PN is the entire PN space.

The drawbacks to this architecture include lack of flexibility. It is optimal in hardware and time only for the limited circumstances set forth above. The hardware will be underutilized whenever desired C is less than the number of taps, N, or when the window to be searched, L, is less than the entire PN space and M is greater than one. In the first instance, the delay elements and PN taps exist in hardware whether or not they are used. In the second instance, the entire PN sequence must cycle through before a second non-

coherent energy value is calculated. Furthermore, extra memory is required to store all the partial accumulations for each offset.

For some numerical examples, assume the PN space, PN, is 30000. We will compare a matched filter searcher as described with N=100 delay elements. Assume first that the desired search window also is 30,000, the desired C is 100, and the desired M is 1. These conditions are optimal for the matched filter searcher so its hardware will be fully utilized. The required search time will be L*M =30,000. The serial correlator searcher described above will also utilize its hardware efficiently, but its search time will be L*M*C = 3,000,000, or 100 times greater. So to equal the speed performance with serial correlators, we would need to implement 100 of them in parallel. This would not be as efficient in area as the matched filter.

Now assume that with the same hardware we wish to search a window smaller than the entire PN sequence: L=1000. Assume further that coherent integrations, C, are set to only 25. Let M continue to be 1. This case demonstrates that the matched filter will not utilize all of its hardware efficiently, since 3/4 of it will be unused. The overall search time, 1000, is still lower than that of the serial correlator, 1000*25 = 25,000, but it is only 25 times faster. This assumes that the taps can be programmed in such a way as to take advantage of the reduced window size - with fixed taps this is not the case and the search time will remain 30,000 which is actually slightly slower.

Finally, change only the assumption that M=5. Now the matched filter searcher will continue to operate at 25% hardware efficiency, and it will take M*PN or 150,000 cycles to search (and additional memory is required to store the L partial accumulations). The serial correlator will continue to operate at 100% hardware efficiency and will complete the task in L*C*M or 125,000. Clearly, as M is increased from 5, the performance gains of the serial correlator will only increase.

There are clear benefits in reducing search times ranging from initial acquisition to base-station handoff to multipath demodulation. There is a need in the art for a searcher which combines fast searching with flexibility and hardware efficiency.

SUMMARY OF THE INVENTION

A novel and improved method and apparatus for searching is described. In accordance with one embodiment of the invention, the searcher adds flexibility to the parallel computation features of a matched filter, allowing a variable number of coherent accumulations and a variable number of non-coherent accumulations to be performed at high speed for a wide range of search hypotheses in a resource efficient manner. This exemplary embodiment of the invention allows for parallel use of the matched filter structure in a time-sliced manner to search multiple windows. In addition, the searcher allows for optional independent Walsh decovering for each search window. The time-sharing approach allows for optional frequency searching of any offset.

In the exemplary embodiment, the I and Q channel data are despread utilizing a matched filter structure. The in-phase and quadrature amplitudes of the despreading delivered to coherent accumulators to sum for a programmable duration of time. The amplitude accumulations are squared and summed to produce an energy measurement. The energy measurement is accumulated for a second programmable time to perform non-coherent accumulation. The resulting value is used to determine the likelihood of a pilot signal at that offset.

Each matched filter structure comprises an N-value shift register for receiving data, a programmable bank of taps to perform despreading and optional Walsh decovering, and an adder structure to sum the resulting filter tap calculations. The matched filter structure can optionally be used in a time-sharing manner to search multiple windows as dictated by a multiplexor which supplies various streams of tap values for despreading (with optional Walsh decovering included in the tap values). In addition, an optional phase rotator can be added to apply multiplexed phase values to perform frequency searching. Every cycle the matched filter structure produces an intermediate calculation for a particular offset (with optional Walsh decovering and optional phase rotation) which includes N calculations based on the data in the shift register. Masking features may be used to allow a calculation using less than N values to be performed). The identification of certain features as optional does not imply that other features are required. Different aspects of the invention may be incorporated or omitted in different embodiments.

BRIEF DESCRIPTION OF THE DRAWINGS

The features, objects, and advantages of the present invention will become more apparent from the detailed description set forth below when taken in conjunction with the drawings in which like reference characters identify correspondingly throughout and wherein:

FIG. 1 is a block diagram of cellular telephone system;

FIG. 2 is a block diagram of a prior art serial correlator searcher;

FIG. 3 is a block diagram of a prior art matched filter searcher;

FIG. 4 is a block diagram configured in accordance with the exemplary embodiment of this invention;

FIG. 5 depicts a QPSK despreader;

FIG. 6 depicts a BPSK despreader; and

FIG. 7 is a more detailed block diagram configured in accordance with the present invention;

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

A block diagram configured in accordance with the one embodiment of the invention as shown in FIG. 4. I and Q data (Hereinafter D_I and D_Q) enters shift registers **400** and **402**, respectively. The size of the matched filter component of this invention is given by N, the number of memory locations in the shift registers. Data is continually loaded and shifted through the shift registers at a constant rate. In the exemplary embodiment, data is loaded in at twice the chip rate. This allows for searching on every chip and half-chip boundary.

The data in shift registers **400** and **402** are then correlated with N-bit portions of the I and Q PN sequences (Hereinafter PN_I and PN_Q) which are loaded into despreader **410**. To despread a QPSK spread pilot signal, complex despreading is performed: $(D_I + jD_Q)\bullet(PN_I + jPN_Q) = (D_IPN_I + D_QPN_Q) + j(D_QPN_I - D_IPN_Q)$. FIG. 5 depicts one stage of the N-stage QPSK despreader. One of the N values of D_I is multiplied by the corresponding tap value PN_I in multiplier **600** and by the corresponding tap value PN_Q in multiplier **604**. Similarly, D_Q is multiplied by tap values PN_I and PN_Q in multipliers **604** and **606**, respectively. The output of multipliers **600** and **606** are summed in adder **608**. The output of multiplier **604** is subtracted from the output of multiplier **602** in adder **610**. The

output of adder **608** is the despread I value. The output of adder **610** is the despread Q value. Since there are N stages, there will be N such complex results.

The present invention is also useful for BPSK despreading. In this case there is only a single PN sequence to correlate with, which provides the tap values for both the I and Q in despreader **410**. The circuit shown in FIG. 5 can be used as is with the single PN sequence being delivered to both PN_I and PN_Q. FIG. 6 shows the simplified despreader which can be used if only BPSK despreading is desired. D_I and D_Q are multiplied by the PN sequence in multipliers **612** and **614** respectively. The results are summed in adder **616** to produce the despread I value. The output of multiplier **612** is subtracted from multiplier **614** in adder **618** to produce the despread Q value. Again there are N stages, so there will be N complex results.

Although FIG. 5 and FIG. 6 show multipliers in use, simplifications are known in the art. When the tap values are binary, as they are in the exemplary embodiment, consisting only of the values 1 and -1, and the proper data format is chosen for D_I and D_Q, the despreading step can be accomplished utilizing only XOR gates and multiplexors (details not shown).

Referring again to Fir. 4, the N despread I and despread Q values produced in despreader **410** are summed respectively in summers **420** and **422**. Each time the data in shift registers **400** and **402** change, new sums are calculated in summers **420** and **422**. Each sum is an N-chip coherent accumulation of a particular offset. The process is repeated for a programmable number of cycles without changing the tap values in despreader **410**. For example, in the exemplary embodiment the matched filter size, N, is 64. Suppose a search window size, L, of 64 and a coherent accumulation, C, of 256 was desired. In this case, the tap values appropriate for the beginning of the window are loaded into despreader **410** and data is cycled through the shift register, producing results from summers **420** and **422** each cycle.

Each result is loaded into coherent accumulators **430** and **432**, respectively. These accumulators accommodate multiple accumulations at a single time. In the exemplary embodiment, they are RAM based. During each cycle, the appropriate partial accumulation is retrieved, added to the output of either summer **420** or **422**, and the resultant partial accumulation is stored again in the RAM. In our example, when 64 cycles have passed, the first 64 I and Q sums have been loaded into accumulators **430** and **432**. Each of these sums corresponds to a C of 64, since that is the width of the matched filter.

During this time, a new set of tap values for despreader **410** have been calculated. These are calculated so that the same 64 offset hypotheses that were tested in the first pass can be tested again. If the tap values were not changed, a new offset would be tested with each cycle until the entire PN space had been searched (like a standard matched filter searcher described above). The matched filter procedure is repeated again for another 64 cycles. This time, each result is summed with the corresponding partial accumulation for its offset as stored in accumulators **430** and **432**. After 64 cycles have passed, each partial accumulation is made up of two 64 chip partial accumulations, corresponding to a C of 128. The process is repeated twice more, changing the taps each time until the accumulators have accumulated four 64 chip values for the desired C of 256. In this configuration, the searcher can perform coherent accumulation on any C that is an integer multiple of N. The window size that can be concurrently searched is determined by the number of partial accumulations which can be stored in accumulators **430** and **432**. (The upper bound on C is determined by the number of bits of precision employed and scaling techniques used, if any. Those skilled in the art can readily design circuits which accommodate a desired C value.)

The loading of PN tap values is performed as follows: the PN sequences will be generated differently depending on whether the same set of hypotheses is to be tested or a new set is beginning. In the exemplary embodiment, the PN sequences are generated via linear feedback shift register (LFSR) based PN generators. The timing of tap generation is best explained with an example. In the exemplary embodiment, the matched filter is N values wide so an N bit tap sequence must be generated. For simplicity we will assume that data changes at the chip rate which is the same rate the PN generators must be updated. This is in contrast to the exemplary embodiment in which data is updated at twice the chip rate, so two data samples are correlated with each PN state. Suppose that we wish to accumulate C=192 values for a window size of 128. Assume our PN generator has generated the appropriate first 64 I and Q tap values which are loaded into despreader **410**. 64 sets of data will cycle through shift registers **400** and **402**. For each set a 64 value coherent I sum is calculated and stored in non-coherent accumulator **430** and a 64 value coherent Q sum is calculated and stored in accumulator **432**. Each coherent sum corresponds to one of the first 64 sequential offset hypotheses being searched. Since a C of 192 is desired, the above 64 cycles must be repeated 3 times to reach 192. But appropriate steps must be taken to properly align the PN taps in despreader **410** to the incoming data. We desire that the same offsets be tested again to

produce the second set of coherent values. The PN generators used to create the incoming data have moved forward 64 chips. We also need to load a new set of PN values 64 chips forward to retest the same offsets. These values are created by the PN generators while the first 64 sums are generated. The process is repeated for the third set to create coherent accumulations of 192 chips.

Now the first half of the search window has been performed. The PN generators used to created the incoming data have moved forward by 64 chips again. If we loaded a similar advanced PN sequence into despreader **410**, we would collect more data on the first 64 offsets, which is not needed in this example. Instead, we wish to introduce an offset of 64 to test the next 64 offsets. We can do this by simply not updating the PN values (since the PN sequence in the incoming data has advanced in relation to the values presently in despreader **410**). When the first 64 calculations are performed for the second half of the window, a new set of PN values must be loaded in despreader **410** to collect more data on the same offsets, just as described above. The process repeats until 192 chips worth of data have been accumulated.

When the coherent accumulations of the I and Q data are complete as just described, the resultant values are squared and summed (I^2 + Q^2) as shown in energy calculator **440**. The result for each offset is loaded into non-coherent accumulator **450**. This accumulator is a multi-accumulation capable accumulator similar to accumulators **430** and **432**. For the programmed number of non-coherent accumulations, M, the values of independent coherent accumulations are accumulated for each offset in the search window. Each time the energy is stored in non-coherent accumulator **450**, the partial accumulations in coherent accumulators **430** and **432** are reset for another C calculations.

Those skilled in the art will employ myriad solutions to process the results stored in non-coherent accumulator **450**. In the exemplary embodiment, the results of non-coherent accumulator **450** are delivered to DSP **460** where the values are examined to determine which offset in the search window, if any, likely corresponds to the location of a pilot signal. DSP **460**, which can be any DSP or microprocessor capable of performing the desired operations, can control all of the matched filter searching procedures. It may be dedicated to the searcher, or the search functions may make up just a fraction of the various tasks that DSP **400** performs in the operation of the subscriber unit. The entire process as just described can be repeated for multiple search windows if necessary.

FIG. 5 depicts the exemplary embodiment of the present invention. A received signal is collected by antenna **501**. The received signal is processed in

a receiver labeled RX_IQ_DATA **500**. The receiver performs all processing necessary to provide an I and Q data stream in digital form sampled at eight times the chip rate. A variety of other sampling rates could also be used, as known in the art. These samples can then be delivered through mux **504** to subsampler **506** where the chipx8 rate I and Q sample streams are reduced to chipx2 streams which is the rate chosen among other possibilities for the exemplary embodiment. The chipx2 I and Q data streams are then fed to mux **508**.

Sample RAM **502** and muxes **504** and **506** make up a data source option. I and Q samples can be stored in sample RAM **502** at the chipx8 rate or at chipx2. Chipx8 rate streams can subsequently be delivered through mux **504** to subsampler **506** as described above. Alternatively, chipx2 streams can bypass subsampler **506** through mux **508**. Clearly, less RAM storage is required to store chipx2 data than to store chipx8 data. This data source option is not mandatory to practice the present invention. It adds the extra benefit of being able to process data while the rest of the receiver or mobile station is in a low-power or idle mode. Multiple search windows of offset hypotheses can be tested on the same group of sampled data. As long as the results are generated before external conditions have changed so as to make them stale, this procedure can generate power savings. Sample RAM **502** can optionally be loaded with values other than those from receiver **500**. It is also possible to utilize the stored data from sample RAM **502** for other demodulation activities (for which chipx8 rate sampling may be appropriate). It is conceivable that sample RAM **502** will be loaded for later additional processing while simultaneously performing a search on the samples being stored.

Gain **510** is an optional block for providing any amplification which may be necessary. Rotator **512** is another option to be added in situations where a frequency offset exists whose removal is desired. The results are delivered to N-bit shift register **514**. It should be clear from the previous paragraphs that any combination or none of the aforementioned options are required to practice this invention. The I and Q data streams can be directly delivered to N-bit shift register **514**. Furthermore, to perform QPSK despreading and coherent searching it is clear that circuitry for both an I and Q path needs to be employed (or equivalent time-sharing) as was shown in FIG. 4. For simplicity and clarity the I and Q paths will be shown as a single path. For example, N-bit shift register **514** is comprised of 2 N-bit storage elements, one for the I values and a second for the Q values.

The I and Q samples are then delivered to QPSK despreader **518**. The samples are despread with PN sequences delivered through mux **516**. The present invention lends itself well to parallel utilization through time-sharing. Four different PN streams with optional Walsh covering are shown as inputs to mux **516**. In the exemplary embodiment, the circuits are operating at an internal clock rate of eight times the chip rate (chipx8). As stated above, the I and Q samples are delivered at a rate of chipx2. This allows for searches to be performed of offsets in between each chip as well as on chip boundaries. As such, the matched filter hardware can be utilized 4 times for each set of data. Therefore, four different PN sequences can be used to search 4 different windows simultaneously (or a single PN sequence with 4 different Walsh codes, or any combination thereof). By increasing the system clock in relation to the data rate, greater or fewer windows can be searched simultaneously.

The despread values are shown entering mask block **519**. This is an optional block which can be used to allow less than N coherent calculations to be performed. For example, in the exemplary embodiment, N is set to 64. If only C=32 was desired, the mask could be set to zero out 32 of the 64 results. This is also convenient when deploying this invention with legacy algorithms. Suppose an algorithm is set to require C of 152, for example. The mask can be disabled for 2 iterations of 64 value calculations. The remaining 152-128 = 24 chips worth of data can be added by setting the mask accordingly. It will be obvious to those skilled in the art that alternative mask locations are possible to perform the same function, including zeroing out the data in the N-bit shift register **514**. (The mask can optionally be applied further down the adder tree at the cost of resolution).

The resulting N I values and N Q values will be delivered to adder tree **520**, where a total I sum and a total Q sum will be calculated. A typical adder tree is shown in FIG. 5, but any adder structure can be employed to perform the sum (for example, a serial adder running faster than the matched filter).

Mux **522** and phase rotator **524** make up another option which can enhance the present invention. Up to four different phase values, θ_0, θ_1, θ_2, and θ_3 can be included through mux **522** and rotator **524**. This allows frequency searching of four frequencies on a phase offset hypothesis. Of course, fewer or greater frequencies can be searched if the system clock choice provides fewer or greater spare cycles in relation to the incoming I and Q data rate. The total number of frequency searches and PN searches utilizing mux **516** can not be greater than the number of spare cycles for a single matched filter structure. For example, in the exemplary embodiment data is updated at a rate of chipx2.

The system clock runs at chipx8, so there are 4 cycles to utilize. Any combination of 4 searches can be performed for each set of data. For example, a single PN sequence can be used for all despreading in despreader **518**. Then four different frequencies can be searched. Alternatively, a single frequency can be searched and four different PN/Walsh combinations can be searched, or 2 different PN/Walsh combinations can be searched with 2 different frequencies, or 4 different PN/Walsh combinations each having a different frequency, and so on.

As described in relation to FIG. 4, the results from the matched filter must be coherently accumulated. The exemplary embodiment's coherent accumulator is made up of items **526-540** in FIG. 7. Those skilled in the art will recognize that there are a variety of means to produce accumulators which can easily be substituted to enable the present invention. Mux **526** and gates **528** and **540** show one method to effect the timing. Four searches can be performed for each cycle of incoming data. The accumulations of each of these need not be time aligned, so provision is made to start each of the four accumulations by the inputs to mux **526**: start_co_accum0 - start_co_accum3. When any of these signals is asserted, the value from rotator **524** will be added in adder **530** to zero, which effectively resets that accumulation. Otherwise, the partial accumulation will be added to the value from rotator **524** in adder **530** as taken from mux **538**, described shortly.

Items **532-538** make up the exemplary storage element of the accumulator. The storage element needs to be able to be written to and read from during each cycle. A dual port RAM could be employed, as could a single port RAM being accessed at twice the cycle rate. Two single port rams alternately read and written could accomplish the task as well. Or, single port coherent RAM **534** can be deployed as shown. Since there is always a delay between the time a particular partial accumulation is stored and when it needs to be accessed, buffering can be used to allow the RAM to alternately be read or written in each cycle. The RAM width will be twice the width of a partial accumulation. One partial accumulation is stored in buffer **532** while coherent RAM **534** is read. The read data will comprise two partial accumulations, the first of which is stored in buffer **536**, the second of which proceeds through mux **538** to gate **528** as described above. In alternating cycles, the partial accumulation from adder **530** along with one stored in buffer **532** will be written to coherent RAM **534**. Since no data is available to be read, mux **538** will select the partial accumulation from buffer **536** to supply to gate **528**. This procedure is known as double packing.

The same start signal coming from mux **526** controls the output of the final coherent accumulations. When the accumulation is not starting, gate **540** will be disabled such that its output will be zero. When a new accumulation is beginning, which corresponds to the prior being completed, the value from mux **538** is supplied through gate **540** to energy calculator **542** (note that gate **528** simultaneously prevents this value from entering summer **530**). Remember that there exists both an I and Q path up until this point, so energy accumulator **542** receives an I and a Q value from two coherent accumulators, even though only one is shown in FIG. 5 for clarity. The I value is squared and added to the squared Q value and the result is presented to summer **548**. Note that the output of energy accumulator **542** is zero for all cycles but one per coherent accumulation period.

Items **544** - **558** make up a single non-coherent accumulator (I and Q are now merged) which is identical to the accumulators described above. Summer **548** supplies partial accumulations of energy values to a double-packed RAM comprised of buffer **550**, non-coherent RAM **552**, buffer **554**, and mux **556**. The timing control is effected similarly through mux **544** and signals start_nc_accum0 - start_nc_accum3 in conjunction with gates **546** and **558**.

The results of the non-coherent accumulations, as passed through gate **558**, are the energy values associated with each offset hypothesis. As described above, the entire structure can be controlled via a microprocessor or DSP as shown in block **564**. The values can be used to determine the location of a pilot, by, for example, comparing each value to a predetermined threshold.

In the exemplary embodiment, peak detector **560** receives the energy values for the hypotheses. The peak detector is used to suppress the above-threshold energy value which is a half chip apart from the energy peaks. The algorithm for peak detection is as follows. For E(n), defined as the energy at the nth offset, a peak is detected if the following is true:

$$E(n-1) < E(n) \quad \text{AND} \quad E(n) >= E(n+1) \qquad (1)$$

The energy values at window boundaries may be saved and further filtered to remove potential false peaks at the borders. This may be done in additional back end filters, potentially in DSP **564**. The remaining peaks after peak filtering are delivered to sorting queue **562**. Sorting queue **562** is used to generate four to eight maximum values for each search window. Each energy value and its associated PN position (or offset) are stored in the queue. DSP **564**

is notified through interrupt when a window search is complete and given access to the values stored in the sorting queue.

The present invention provides a great deal of flexibility, much of which has already been described. Recall the variables L, C, M and N (number of hypotheses, coherent accumulations, non-coherent accumulations, and number of taps, respectively) from prior discussion. Include the additional variable for frequency searching, f. In order to increase searcher throughput, the clock rate can be increased from that given in the exemplary embodiment. The throughput scales directly with the clock rate. Define the T as the number of time-sharing cycles available for parallel use of the architecture due to clock rate scaling. This invention allows for any combination of searches given by the product, LCMf, equal to the total number of cycles a serial correlator would have to perform to accomplish such a search. This invention can perform the search at a much greater rate: LCMf/NT.

There is also scalability at the architectural level of any particular implementation of this invention. For approximately the same amount of hardware, a number of configurations can be deployed depending on what sort of searching characteristics are desired.

Following are three example configurations each including approximately the same complexity (and in this case assuming the same clock rate in each: data changing at chipx2 and system clock of chipx8). One option is to utilize a single register of size N = 32 shared by four matched filters of size N=32 (each of the four matched filters containing four parallel searchers via time-multiplexing as shown in FIG. 5). This option provides a minimum C = 32, minimum L = 64, and the number of parallel searchers, S = 16. A second option is to use a single register of size N = 64 and two parallel N=64 matched filters. Here the minimum C = 64, minimum L = 128, and S = 8. A third comparably sized option is to use one N=128 searcher as shown in FIG. 5. Here minimum C = 128, minimum L = 256, with S = 4. These three examples are not meant to be exhaustive but serve to illustrate a few of the potential embodiments of the present invention.

Thus, a method and apparatus for a programmable matched filter searcher has been described. The description is provided to enable any person skilled in the art to make or use the present invention. The various modifications to these embodiments will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other embodiments without the use of the inventive faculty. Thus, the present invention is not intended to be limited to the embodiments shown herein but is

to be accorded the widest scope consistent with the principles and novel features disclosed herein.

We claim:

CLAIMS

1. A programmable matched filter searcher comprising:
a shift register for receiving sets of incoming data;
a PN generator for generating PN sequences;
a loadable matched filter for loading said PN sequences, despreading said sets of incoming data and summing the intermediate results; and
an accumulator for receiving said sums and accumulating them in sets to produce a set of accumulated sums.

2. A programmable matched filter searcher comprising:
a shift register for receiving sets of incoming in-phase(I) data;
a shift register for receiving sets of incoming quadrature(Q) data;
a PN generator for generating PN sequences;
a matched filter having:
a despreader for receiving said sets of I data, said sets of Q data, and said PN sequences and for producing sets of despread I values and producing sets of despread Q values;
a summer for summing said sets of despread I values to produce I sums;
a summer for summing said sets of despread Q values to produce Q sums;
an I accumulator for receiving said I sums and accumulating them in sets to produce a set of accumulated I sums;
a Q accumulator for receiving said Q sums and accumulating them in sets to produce a set of accumulated Q sums; and
an energy calculator for receiving sets of accumulated I sums and sets of accumulated Q sums, squaring respective ones of sets of accumulated I sums, squaring respective ones of sets of accumulated Q sums, and summing the results of said squares of respective ones of sets of I and Q sums to produce sets of energy values.

3. The programmable matched filter searcher of Claim 2 further comprising an accumulator for receiving said sets of energy values and producing sets of accumulations of ones of said sets of energy values.

4. The programmable matched filter searcher of Claim 3 wherein:
I and Q PN sequences are produced by said PN generator; and

said despreader performs QPSK despreading.

5. The programmable matched filter searcher of Claim 3 wherein said despreader performs BPSK despreading.

6. The programmable matched filter searcher of Claim 3 further comprising a multiplexor for receiving multiple PN sequences and delivering them for time-sharing of said loadable matched filter to produce additional sets of sums based on said multiple PN sequences.

7. The programmable matched filter searcher of Claim 3 further comprising:

a multiplexor for receiving one or more phase values; and

I and Q rotators for receiving outputs said I and Q loadable matched filters and rotating said outputs according to the phase output of said multiplexor, and delivering the results to said I and Q accumulators.

8. A method for performing programmable matched filter searching comprising the steps of:

a) storing sets of I and Q data;

b) producing PN sequences;

c) despreading said sets of I and Q data with said PN sequences to produce I and Q despread values;

d) summing results of said despread I values;

e) summing results of said despread Q values;

f) accumulating the resultant summed despread I values;

g) accumulating the resultant summed despread Q values;

h) squaring the accumulated despread I values;

i) squaring the accumulated despread Q values; and

j) summing both said squares.

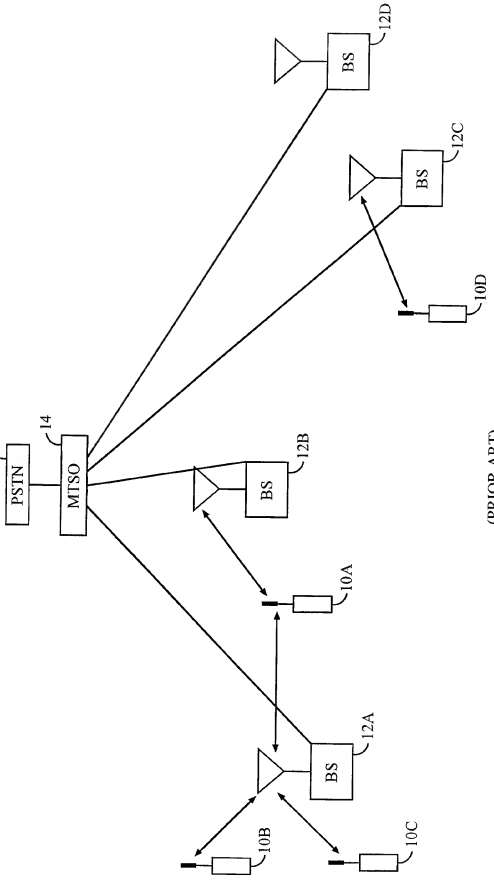
9. The method of Claim 6 further comprising the step of accumulating said sum of squares.

10. A programmable matched filter searcher comprising:

memory for receiving sets of incoming data;

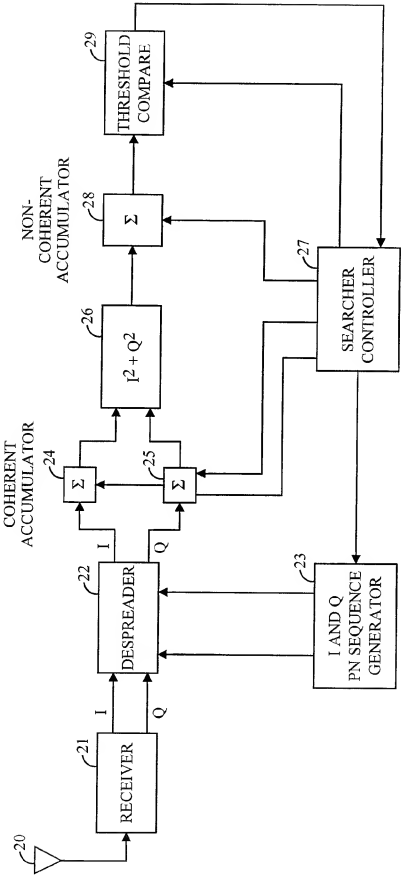
PN generator for generating PN sequences;

loadable matched filter for loading said PN sequences, despreading said sets of incoming data and summing the intermediate results.

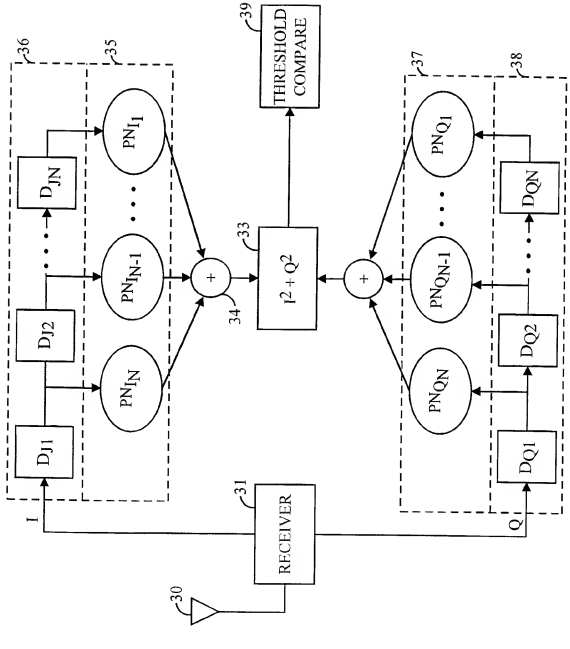


(PRIOR ART)

FIG. 1



(PRIOR ART)
FIG. 2



(PRIOR ART)
FIG. 3

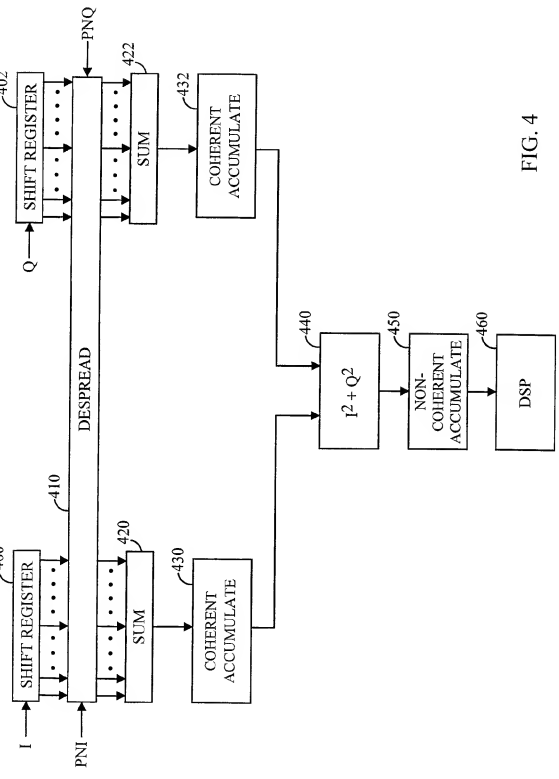

I
PNI
Q
PNQ
400
SHIFT REGISTER
402
SHIFT REGISTER
410
DESPREAD
420
SUM
422
SUM
430
COHERENT ACCUMULATE
432
COHERENT ACCUMULATE
440
$I^2 + Q^2$
450
NON-COHERENT ACCUMULATE
460
DSP

FIG. 4

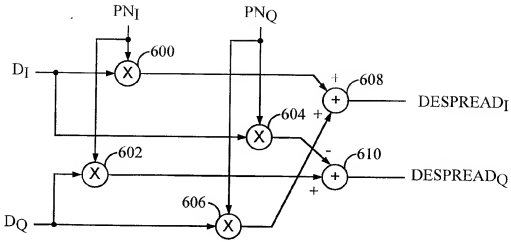

PN_I
PN_Q
600
D_I
608
DESPREAD_I
604
602
610
DESPREAD_Q
606
D_Q

FIG. 5

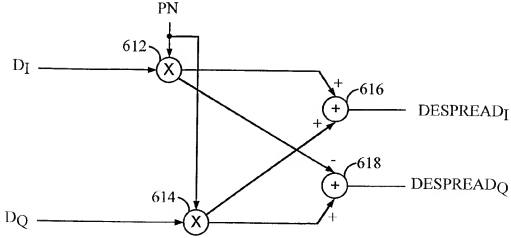

PN
612
D_I
616
DESPREAD_I
618
DESPREAD_Q
614
D_Q

FIG. 6

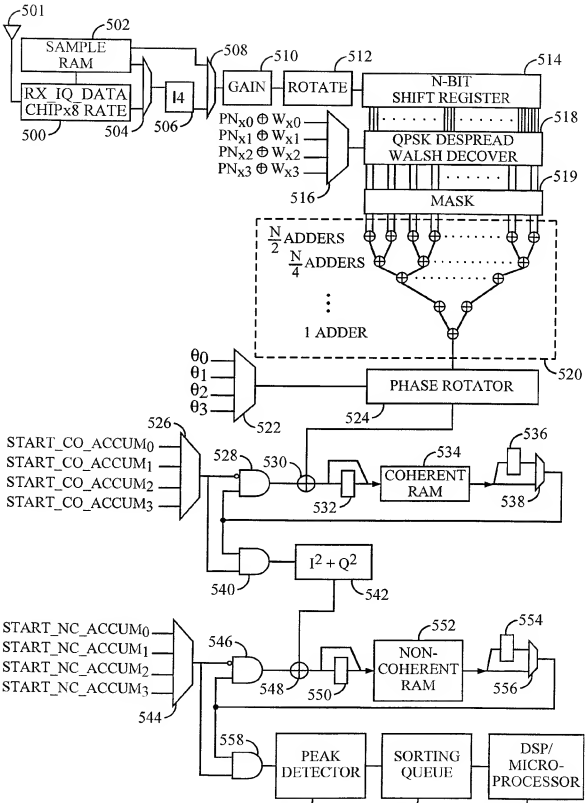

501
502
SAMPLE RAM
RX_IQ_DATA CHIPx8 RATE
500
504
I4
506
508
510
GAIN
512
ROTATE
514
N-BIT SHIFT REGISTER
518
QPSK DESPREAD WALSH DECOVER
519
MASK
516
PNx0 ⊕ Wx0
PNx1 ⊕ Wx1
PNx2 ⊕ Wx2
PNx3 ⊕ Wx3
N/2 ADDERS
N/4 ADDERS
1 ADDER
520
PHASE ROTATOR
524
θ0
θ1
θ2
θ3
522
526
START_CO_ACCUM0
START_CO_ACCUM1
START_CO_ACCUM2
START_CO_ACCUM3
528
530
532
534
COHERENT RAM
536
538
I2 + Q2
540
542
START_NC_ACCUM0
START_NC_ACCUM1
START_NC_ACCUM2
START_NC_ACCUM3
544
546
548
550
552
NON-COHERENT RAM
554
556
558
PEAK DETECTOR
560
SORTING QUEUE
562
DSP/ MICRO-PROCESSOR
564

FIG. 7

INTERNATIONAL SEARCH REPORT

Inte national Application No
PCT/US 00/40075

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H04B1/707

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H04B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
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C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 5 872 808 A (KANTERAKIS EMMANUEL ET AL) 16 February 1999 (1999-02-16) column 2, line 59 -column 4, line 49 column 5, line 50 -column 6, line 56 column 9, line 5 -column 11, line 5 column 14, line 3 - line 34 figures 1,2,6	1,10 2-5,8,9
Y	US 5 577 025 A (SKINNER DECEASED GORDON ET AL) 19 November 1996 (1996-11-19) column 11, line 37 -column 12, line 14 figure 2	2-5,8,9

☐ Further documents are listed in the continuation of box C.

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2 August 2000	08/08/2000

Name and mailing address of the ISA	Authorized officer
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Form PCT/ISA/210 (second sheet) (July 1992)

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Information on patent family members

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		WO 9702663 A	23-01-1997

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(71) Applicant: QUALCOMM INCORPORATED [US/US]; 5775 Morehouse Drive, San Diego, CA 92121-1714 (US).

(72) Inventors: SIH, Gilbert, C.; 7804 Pipit Place, San Diego, CA 92129 (US). ZOU, Qinzhen; 11507 Westview Parkway, San Diego, CA 92126 (US). KANG, Inyup; 5385 Toscana Way, Pat.326, San Diego, CA 92126 (US). FEVRIER, Ian, J.; 9936 Kika Court, #3623, San Diego, CA 92129 (US).

(74) Agents: MILLER, Russell, B. et al.; Qualcomm Incorporated, 5775 Morehouse Drive, San Diego, CA 92121-1714 (US).

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Published

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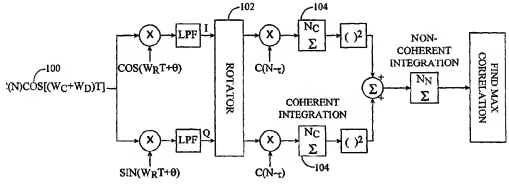
(54) Title: SIMPLIFIED RECEIVER WITH ROTATOR FOR PERFORMING POSITION LOCATION



(57) Abstract

The present invention is a novel and improved method and apparatus for performing position location in wireless communications system. One embodiment comprises a method for performing position location using a set of signals transmitted from a set of satellites including the steps of storing coarse search data, performing a coarse search on said coarse search data for each satellite from said set of satellites, receiving fine search data, performing a set of fine searches on said fine search data, each fine search being performed on a different time segment of said fine search data, and reporting results.

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SIMPLIFIED RECEIVER WITH ROTATOR FOR PERFORMING POSITION LOCATION

BACKGROUND OF THE INVENTION

I. Field of the Invention

The present invention relates to position location. More particularly, the present invention relates to a novel and improved method and apparatus for performing position location in wireless communications system.

II. Description of the Related Art

Both government regulation and consumer demand have driven the demand for position location functionality in cellular telephones. The global positioning system (GPS) is currently available for performing position location using a GPS receiver in conjunction with a set of earth orbiting satellites. It is therefore desirable to introduce GPS functionality into a cellular telephone.

Cellular telephones, however, are extremely sensitive to cost, weight and power consumption considerations. Thus, simply adding additional circuitry for performing GPS location is an unsatisfactory solution for providing position location functionality in a cellular telephone. Thus, the present invention is directed to providing GPS functionality in a cellular telephone system with a minimum of additional hardware, cost and power consumption.

SUMMARY OF THE INVENTION

The present invention is a novel and improved method and apparatus for performing position location in wireless communications system. One embodiment comprises a method for performing position location using a set of signals transmitted from a set of satellites including the steps of storing coarse search data, performing a coarse search on said coarse search data for each satellite from said set of satellites, receiving fine search data, performing a set of fine searches on said fine search data, each

fine search being performed on a different time segment of said fine search data, and reporting results.

BRIEF DESCRIPTION OF THE DRAWINGS

The features, objects, and advantages of the present invention will become more apparent from the detailed description set forth below when taken in conjunction with the drawings in which like reference characters identify correspondingly throughout and wherein:

Fig. 1 is a block diagram of the Global Positioning System (GPS) waveform generator;

Fig. 2 is a highly simplified block diagram of a cellular telephone system configured in accordance with the use of present invention;

Fig. 3 is a block diagram of a receiver configured in accordance with one embodiment of the invention;

Fig. 4 is another block diagram of the receiver depicted in Fig. 3;

Fig. 5 is a receiver configured in accordance with an alternative embodiment of the invention;

Fig. 6 is a flow chart of the steps performed during a position location operation;

Fig. 7 is a block diagram of a DSP configured in accordance with one embodiment of the invention;

Fig. 8 is a flow chart illustrating the steps performed during a search performed in accordance with one embodiment of the invention;

Fig. 9 is a time line illustrating the phases over which fine and coarse searches are performed in one embodiment of the invention;

Fig. 10 is a time line of the search process when performed in accordance with one embodiment of the invention;

Fig. 11 is a diagram of search space.

Fig. 12 is a block diagram of a receiver in accordance with another embodiment of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

A novel and improved method and apparatus for performing position location in wireless communications system is described. The

exemplary embodiment is described in the context of the digital cellular telephone system. While use within this context is advantageous, different embodiments of the invention may be incorporated in different environments or configurations. In general, the various systems described herein may be formed using software controlled processors, integrated circuits, or discreet logic, however, implementation in an integrated circuit is preferred. The data, instructions, commands, information, signals, symbols and chips that may be referenced throughout the application are advantageously represented by voltages, currents, electromagnetic waves, magnetic fields or particles, optical fields or particles, or a combination thereof. Additionally, the blocks shown in each block diagram may represent hardware or method steps.

Fig. 1 is a block diagram of the Global Positioning System (GPS) waveform generator. The circle with a plus sign designates modulo-2 addition. In general, the GPS constellation consists of 24 satellites: 21 space vehicles (SVs) used for navigation and 3 spares. Each SV contains a clock that is synchronized to GPS time by monitoring ground stations. To determine a position and time, a GPS receiver processes the signals received from several satellites. At least 4 satellites must be used to solve for the 4 unknowns (x, y, z, time).

Each SV transmits 2 microwave carriers: the 1575.42 MHz L1 carrier, which carries the signals used for Standard Positioning Service (SPS), and the 1227.60 MHz L2 carrier, which carries signals needed for Precise Positioning Service (PPS). PPS is used by governmental agencies and allows a higher degree of accuracy in positioning.

The L1 carrier is modulated by the Coarse Acquisition (C/A) code, a 1023-chip pseudorandom code transmitted at 1.023 Mcps that is used for civil position location services. (The Coarse Acquisition code should not be confused with the coarse and fine acquisitions described herein, which both involve the use of the C/A codes.) Each satellite has its own C/A code that repeats every 1ms. The P code, which is used for PPS, is a 10.23 MHz code that is 267 days in length. The P code appears on both carriers but is 90 degrees out of phase with the C/A code on the L1 carrier. The 50Hz navigation message, which is exclusive-ORed with both the C/A code and P code before carrier modulation, provides system information such as satellite orbits and clock corrections.

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Each satellite has a different C/A code that belongs to a family of codes called Gold codes. Gold codes are used because the cross-correlation between them are small. The C/A code is generated using two 10-stage shift registers as shown below in figure 1.4-2. The G1 generator uses the polynomial $1+X^3+X^{10}$, while the G2 generator uses the polynomial $1+X^2+X^3+X^6+X^8+X^9+X^{10}$. The C/A code is generated by exclusive ORing the output of the G1 shift register with 2 bits of the G2 shift register.

Fig. 2 is a highly simplified block diagram of a cellular telephone system configured in accordance with the use of present invention. Mobile telephones **10** are located among base stations **12**, which are coupled to base station controller (BSC) **14**. Mobile switching center MSC **16** connects BSC **14** to the public switch telephone network (PSTN). During operation, some mobile telephones are conducting telephone calls by interfacing with base stations **12** while others are in standby mode.

As described in copending US patent application serial no. 09/040,051 entitled "SYSTEM AND METHOD FOR DETERMINING THE POSITION OF A WIRELESS CDMA TRANCEIVER" assigned to the assignee of the present invention and incorporated herein by reference, position location is facilitated by the transmission of a position request message containing "aiding information" that allows the mobile telephone to quickly acquire the GPS signal. This information includes the ID number of the SV (SV ID), the estimated code phase, the search window size around the estimate code

phase, and the estimated frequency Doppler. Using this information, the mobile unit can acquire the GPS signals and determine its location more quickly.

In response to the aiding message, the mobile unit tunes to the GPS frequency and begins correlating the received signal with its locally generated C/A sequences for the SVs indicated by the base station. It uses the aiding information to narrow the search space and compensate for Doppler effects, and obtains pseudo-ranges for each satellite using time correlation. Note that these pseudo-ranges are based on mobile unit time (referenced from the CDMA receiver's combiner system time counter), which is a delayed version of GPS time.

Once this information is calculated, the mobile unit sends the pseudo-ranges for each satellite (preferably to 1/8 chip resolution) and the time the measurements were taken to the base station. The mobile unit then retunes to CDMA to continue the call.

Upon, receipt of the information, the BSC uses the one-way delay estimate to converts the pseudo-ranges from mobile unit time to base station time and computes the estimated position of the mobile unit by solving for the intersection of several spheres.

Another parameter provided by the aiding message is the frequency Doppler or Doppler offset. The Doppler effect manifests as an apparent change in the frequency of a received signal due to a relative velocity between the transmitter and receiver. The effect of the Doppler on the carrier is referred to as frequency Doppler, while the effect on the baseband signal is referred to as code Doppler.

In the GPS case, frequency Doppler changes the received carrier frequency so the effect is the same as demodulating with a carrier offset. Since the base station's GPS receiver is actively tracking the desired satellite, it knows the frequency Doppler due to satellite movement. Moreover, the satellite is so far away from the base station and the mobile unit that the Doppler seen by the mobile unit is effectively the same as the Doppler seen by the base station. In one embodiment of the invention, to correct for the frequency Doppler value, the mobile unit uses a rotator in the receiver. The frequency Doppler ranges from -4500Hz to +4500Hz, and the rate of change is on the order of 1 Hz/s.

The effect of the code Doppler is to change the 1.023Mhz chip rate, which effectively compresses or expands the width of the received C/A code chips. In one embodiment of the invention, the mobile unit correct for code

Doppler by multiplying the frequency Doppler by the ratio 1.023/1575.42. The mobile unit can then correct for code Doppler over time by slewing (introducing delay into) the phase of the received IQ samples in 1/16 chip increments as necessary.

Fig. 3 is a block diagram of the receiver portion of a cellular telephone (wireless subscriber unit) configured in accordance with one embodiment of the invention. The received waveform **100** is modeled as the C/A signal c(n) modulated with a carrier at frequency $w_c + w_d$, where w_c is the nominal carrier frequency 1575.42 MHz, and w_d is the Doppler frequency created by satellite movement. The Doppler frequency ranges from 0 when the satellite is directly overhead, to about 4.5kHz in the worst case. The receiver analog section can be modeled as demodulation with a carrier at frequency w_r and random phase _, followed by low pass filtering.

The resulting baseband signal is passed through an A/D converter (not shown) to produce digital I and Q samples, which are stored so that they may be repeatedly searched. The samples are generated at two times the C/A code chip rate (chipx2) which is a lower resolution than necessary to perform the fine search algorithm, but which allows 18 ms of sample data to be stored in a reasonable amount of memory. In general, it is desirable to perform the searching over something greater than 10ms in order to allow acquisition in most environmental conditions, with 18ms being a preferred integration period. These environmental conditions include being inside or not having a direct view to the satellite.

During operation, the samples are first rotated by rotator **102** to correct for the Doppler frequency offset. The rotated I and Q samples are correlated with various offsets of the satellite's C/A sequence and the resulting products are coherently integrated over Nc chips by integrators **104**. The coherent integration sums are squared and added together to remove the effect of the unknown phase offset _. To augment the hypothesis test for a particular offset, several coherent intervals are non-coherently combined. This despreading is performed repeatedly at various time offsets to find the time offset of the satellite signal. Rotator **102** removes the frequency Doppler created by satellite movement. It uses the Doppler frequency specified by the base station (preferably quantized to 10Hz intervals) and rotates the I and Q samples to remove the frequency offset.

In one embodiment of the invention, the rotation is continuous only over the coherent integration window. That is, the rotator stops in between

coherent integration periods of, for example, 1 ms. Any resulting phase difference is eliminated by the square and sum.

Fig. 4 is another block diagram of a receiver configured in accordance with one embodiment of the invention, where the rotator portion of the receiver is depicted in greater detail.

Fig. 5 is a receiver configured in accordance with an alternative embodiment of the invention. This internal embodiment of the invention takes advantage of the ability to stop the rotator between coherent integration periods by rotating the locally generated C/A sequence instead of the input samples.

As shown, the C/A sequence c(n) are rotated by application to the sinusoids $\sin(W_d n T_c)$ and $\cos(W_d n T_c)$ and then stored. The rotation of the C/A sequence only needs to be done once for each satellite. Thus, rotating the C/A sequence reduces the amount of computation required. It also saves memory in the DSP used to perform this computation in one embodiment of the invention.

Another significant impairment that degrades the performance of the position location algorithm is the frequency error in the mobile units internal clock. It is this frequency error which drives the use of short coherent integration times on the order of 1 ms. It is preferable to perform coherent integration over longer time periods.

In an exemplary configurations, the mobile's free running (internal) local oscillator clock is a 19.68MHz crystal that has a frequency tolerance of +/-5ppm. This can cause large errors on the order of +/- 7500 Hz. This clock is used to generate the carriers used for demodulation of the GPS signals, so the clock error will add to the signal acquisition time. Because the time available to search is very small, error of this magnitude due to the frequency tolerance are not tolerable and must be greatly reduced.

To allow longer coherent integration times, in one embodiment of the invention, the CDMA receiver corrects for local oscillator error by using timing acquired from the CDMA pilot, or any other source of timing information available. This produces a control signal that is used to tune the local oscillator clock to 19.68MHz as closely as possible. The control signal applied to the local oscillator clock is frozen when the RF unit switches from CDMA to GPS.

Even after the correction is performed using the timing information from the bases station (or other source), however, some additional clock error remains. In one embodiment of the invention, the resulting frequency

uncertainty after correction is +/- 100Hz. This remaining error still reduces the performance of the receiver, and in general prevents longer coherent integration times. In one embodiment of the invention, the remaining error simply avoided by performing non-coherent integration for duration of more than 1ms which reduces performance.

As also shown in **Fig. 1**, the 50Hz NAV/system data is also modulated onto the L1 carrier. If a data transition (0 to 1 or 1 to 0) occurs between the two halves of a coherent integration window, the resulting coherent integration sum will be zero because the two halves will cancel each other out. This effectively reduces the number of non-coherent accumulations by one in the worst case. Although the data boundaries of all the satellites are synchronized, they do not arrive at the mobile unit simultaneously because of the differences in path delay. This path delay effectively randomizes the received data phase.

In one embodiment of the invention, the problem of different data phases on different signals is to include the data phase in the aiding information sent from the base station to the mobile unit. Since the base station is demodulating the 50Hz data, it knows when the data transitions occur for each satellite. By using knowledge of the one-way delay, the base station can encode the data phase in, for example, 5 bits (per satellite) by indicating which one millisecond interval (out of 20) the data transition occurs on.

If the coherent integration window straddles the 50Hz data boundary the coherent integration is divided into two (2) sections. One section preceding the data boundary and one section following the data boundary. For example, if En1 is the coherent integration sum over the window preceding the data boundary the first half of this window and En2 is the coherent integration sum over the window following the data boundary, the mobile unit then selects the maximum (in magnitude) of (En1 + En2) (in case the data stayed the same) and (En1 – En2) (in case the data changed) to account for the phase change. The mobile unit also has the option of performing non-coherent combining of the two halves over this data window or avoiding this data window completely.

In an alternative embodiment of the invention, the mobile unit attempts to find the data transitions without the aiding information from the base station by comparing the magnitude squared of the sum and difference in 1 ms coherent integration.

In one embodiment of the invention, a firmware-based DSP (Digital Signal Processor) approach is used to perform the GPS processing. The DSP receives I and Q samples at a chipx2 (2.046 MHz) or chipx8 (8.184 MHz) rate, and stores a snapshot of 4-bit I and Q samples in its internal RAM.

In the exemplary embodiment, the DSP generates the C/A sequence, performs rotation to eliminate frequency Doppler, and correlates over the search window provided by the base station for each of the satellites. The DSP performs coherent integration and non-coherent combining and slews an IQ sample decimator as necessary to compensate for code Doppler.

To save computation and memory, the initial search is performed using _ chip resolution and a finer search to obtain 1/8 chip (higher) resolution is performed around the best index (or indexes). System time is maintained by counting hardware-generated 1ms interrupts (derived from local oscillator).

Additionally, in one embodiment of the invention, the fine search is performed by accumulating the chipx8 samples (higher resolution) over the duration of one chip at various chipx8 offsets. The correlation codes are applied to the accumulated values yielding correlation values that vary with the particular chipx8 offset. This allows the code offset to be determined with chipx8 resolution.

Fig. 6 is a flow chart illustrating the steps performed to correct for the local oscillator error during a position location procedure when performed in accordance with one embodiment of the invention. At step **500**, it is determined whether the local oscillator has been corrected recently. If not, then the pilot is acquired from the base station, and error of the local oscillator is determined by comparing to the pilot timing at step **502** and a correction signal generated based on that error.

The flow then leads to step **504**, where the correction signal is frozen at the current value. At step **506**, enters GPS mode and performs the position location using the corrected clock. Once the position location has been performed, the mobile unit leaves GPS mode at step **508**.

Fig. 7 is an illustration of a DSP receiver system configured in accordance with one embodiment of the invention. The DSP performs the entire searching operation with minimal additional hardware. DSP core **308**, modem **306**, interface unit **300**, ROM **302** and Memory (RAM) **304** are coupled via bus **306**. Interface unit **300** receives RF samples from an RF unit (not shown) and provides the samples to RAM **304**. The RF samples can be stored at coarse resolution or fine resolution. The DSP core **308** processes

the samples stored in memory using instruction stored in ROM **302** as well as in memory **304**. Memory **304** may have multiple "banks" some of which store samples and some of which store instructions. Modem **700** performs CDMA processing during normal mode.

Fig. 8 is a flow chart of the steps performed during a position location operation. A position location operation begins when the aiding messing is received, and the RF systems is switched to GPS frequencies at step **600**. When the RF is switched to receive GPS, the frequency tracking loop is fixed. The DSP receives aiding information from the phone microprocessor and sorts the satellites by Doppler magnitude.

At step **602**, the coarse search data is stored within the DSP RAM. The DSP receives a few hundred microseconds of input data to set an Rx AGC. The DSP records the system time and begins storing an 18ms window (DSP memory limitation) of chipx2 IQ data in its internal RAM. A contiguous window of data is used to mitigate the effects of code Doppler.

Once the data is stored, a coarse search is performed at step **604**. The DSP begins the coarse (chipx2 resolution) search. For each satellite, the DSP generates the C/A code, rotates the code based on the frequency Doppler, and correlates over the search window specified by the base station, via repeated application of the C/A code to the stored coarse search data. Satellites are processed over the same 18ms data window and the best chipx2 hypothesis that exceeds a threshold is obtained for each satellite. Although a 2ms coherent integration time (with 9 non-coherent integrations) is used in one embodiment of the invention, longer coherent integration times can be used (for example 18ms), although preferably where additional adjustments are made as described below.

Once the coarse search is performed, a fine search is conducted, at step **606**. Before beginning the fine search, the DSP computes the rotated C/A code for each of the satellites. This allows the DSP to process the fine search in real-time. In performing the fine (chipx8 resolution) search, the satellites are processed one at a time over different data.

The DSP first slews the decimator to compensate for code Doppler for the given satellite(s). It also resets the Rx AGC value while waiting for the next 1ms boundary before storing a 1ms coherent integration window of chipx8 samples.

The DSP processes 5 contiguous chipx8 resolution hypotheses on this 1ms coherent integration window, where the center hypothesis is the best hypothesis obtained in the coarse search. After processing the next 1ms

window, the results are combined coherently and this 2ms sum is combined non-coherently for all Nn iterations.

This step (starting from slewing the decimator) is repeated on the same data for the next satellite until all the satellites have been processed. If the code Doppler for 2 satellites is similar in magnitude, it may be possible to process both satellites over the same data to reduce the number of required data sets. In the worst case, 8 sets of 2*Nn data windows of 1ms are used for the fine search.

Finally, at step **608**, the results are reported to the microprocessor and the vocoder process is restarted within the DSP so that the call can continue. The DSP reports pseudoranges to the microprocessor, which forwards them to the base station. After the microprocessor redownloads the vocoder program code into the DSP memory, the DSP clears its data memory and restarts the vocoder.

Fig. 9 is a diagram illustrating the fine search performed after the coarse search. After isolating the best chipx2 phase in the coarse search, the DSP performs a fine search around this phase to gain chipx8 resolution.

The 5 phases to compare in the fine search are shown enclosed by a rectangle. The best chipx2 phase is evaluated again so that comparisons can be made over the same set of data. This also allows the coarse search and fine search to use different integration times. The fine search is performed separately for each satellite because each satellite may have a different value for code Doppler.

Fig. 10 provides a time line of the search process when performed in accordance with one embodiment of the invention. The overall processing time (coarse + fine search) is performed in about 1.324 seconds in one embodiment of the invention, which does interrupt the call, but still allows the call to continue once the search is performed. The total search time of 1.324 seconds is an upper bound, because it assumes that the DSP needs to search all 8 satellites and each satellite has a search window of 68 chips. The probability that the entire 1.324 seconds will be necessary is small, however, due to the geometry of the satellite orbits.

During the first 18ms **80**, IQ sample data is collected at the GPS frequency. During the period **82**, a coarse search is performed internally which could last up to 1.13 seconds, but which will probably terminate early when the satellite signals are identified. Once the coarse search is performed, the C/A codes are computed during time period 84, which takes 24 ms. During time periods **86** the slew value is adjusted for code Doppler

and the Rx AGC is further adjusted. During time periods 88, fine searches are performed on the IQ data samples, with continuous adjustment performed during time periods 86. The use of 18 ms integration times allows code Doppler to be neglected because the received C/A code phase will be shifted by less than 1/16 of a chip. Up to eight sequences of adjustments and fine searches are performed for the up to eight satellites, at which time the position location procedure is complete.

Additionally, in some embodiments of the invention, the phone continues to transmit reverse link frames to the base station while the position location procedure is performed. These frames may contain null information simply to allow the base station to remain synchronized with the subscriber unit, or the frames may contain additional information such as power control commands or information request. The transmission of these frames is preferably performed when GPS samples are not being gathered when the RF circuitry is available, or while the GPS samples are gathered if sufficient RF circuitry is available.

Although the use of 18ms integration time avoids the effects of code Doppler, the transmission of data over the GPS signals at 50Hz rate can cause problems if a data change occurs within the 18ms processing span (as described above). The data change causes the phase of the signal to shift. The 50Hz data boundaries occur at different places for each satellite. The phase of the 50Hz transitions for each satellite have been effectively randomized by the varying path lengths from each satellite to the phone.

In the worst case, if the data bit was inverted in the middle of a coherent integration interval, the coherent integration could be completely wiped out. For this reason, in an alternative embodiment of the invention, the base station must communicate the data transition boundaries for each satellite to the phone (also described above). Preferably, the data transmission boundary is also included in the aiding message transmitted from the base station (such as in a set of five bit messages indicating the millisecond interval during which the transition occurs for each satellite). The phone uses this boundary to split the coherent integration interval for each satellite into 2 pieces and decide whether to add or subtract the coherent integration sums in these 2 intervals. Thus, by also including the data boundary of each GPS signal, the reliability of the location procedure is increased.

In the exemplary embodiment of the invention, any frequency uncertainty creates a loss in Ec/Nt that increases with the coherent

integration time. For example, uncertainty of +/-100Hz, the loss in Ec/Nt increases rapidly as the coherent integration time is increased, as shown in Table I.

Nc	Loss in Ec/Nt
1023 (1ms)	0.14 dB
2046 (2ms)	0.58 dB
4092 (4ms)	2.42 dB
6138 (6ms)	5.94 dB
8184 (8ms)	12.6 dB

Table I.

As also noted above, there is always some unknown frequency offset of the local oscillator in the mobile unit. It is this unknown frequency offset that prevents longer coherent despreading and integration from being performed. Longer coherent would improve processing if the effects of the unknown frequency offset could be reduced.

In one embodiment of the invention, this unknown frequency offset is accounted for by expanding the search space to 2 dimensions to include frequency searches. For each hypothesis, several frequency searches are performed, where each frequency search assumes the frequency offset is a known value. By spacing the frequency offsets, one can reduce the frequency uncertainty to an arbitrarily small value at the expense of added computation and memory. For example, if 5 frequency hypotheses are used, the resulting search space is shown in **Fig. 10**.

For a +/-100Hz frequency uncertainty, which is the typically operating specification of a mobile unit, this configuration reduces the maximum frequency offset to 20Hz (one hypothesis must be within 20Hz of the actual frequency offset). With a 20ms coherent integration time, the loss in Ec/Nt with a 20Hz frequency offset is 2.42 dB. By doubling the number of frequency hypotheses to 10, the frequency uncertainty can be reduced to 10Hz, which causes an Ec/Nt loss of .58dB. However, adding additional hypotheses widens the search space, which increases both the computation and memory requirements.

One embodiment of the invention computes the frequency hypothesis by lumping the frequency offset in with the frequency Doppler,

and computing a new rotated PN code for each frequency hypothesis. However, this makes the number of frequency hypotheses a multiplicative factor in the total computation: 5 frequency hypotheses would mean 5 times as much computation.

Alternatively, since the frequency uncertainty is small compared to the frequency Doppler, the rotation phase can be considered to be constant over a 1ms interval (8% of a period for an 80Hz hypothesis) in another embodiment of the invention. Therefore, by dividing the coherent integration interval up into 1ms subintervals, the integration sums of the subintervals are rotated to reduce the added computations needed to compute the frequency searches by three orders of magnitude. The result is that longer coherent despreading can be performed, and performance improved.

Fig. 12 is a block diagram of a receiver configured in accordance with the use of longer coherent despreading approach. The first set of multipliers **50** compensates for the frequency Doppler by correlating the IQ samples with a rotated C/A code. This is equivalent to rotating the IQ samples before correlation with the unmodified C/A code. Since the frequency Doppler can be as large as 4500Hz, the rotation is applied to every chip. After coherently integrating over a 1ms interval (1023 chips) using accumulators **52**, the second set of multipliers **54** rotates the 1ms integration sums ($_{-I}$ and $_{-Q}$) to implement the frequency hypothesis. The rotated sums are then added over the whole coherent integration interval.

Recall that the frequency Doppler rotation was only computed on 1023 chips to save memory and computation. For coherent integration times longer than 1ms, each coherent integration sum are multiplied by a phase offset to make the phase of the rotation continuous over time. To show this mathematically, the 1ms coherent integration sum with frequency Doppler rotation can be expressed as:

$$S_1 = \sum_{n=1}^{1023} [I(n) + jQ(n)]c(n)e^{-jw_d nT_c} \quad \text{with } _{-I} = \mathrm{Re}\{S_1\} \text{ and } _{-Q} = \mathrm{Im}\{S_1\}$$

where I(n) and Q(n) are the input samples received on the I and Q channels respectively, c(n) is the unrotated C/A code, w_d is the frequency Doppler, and T_c is the chip interval (.9775us). A 2ms coherent integration sum can be expressed as:

$$S(2ms) = \sum_{n=1}^{2046} [I(n) + jQ(n)]c(n)e^{-jw_d nT_c}$$

$$= \sum_{n=1}^{1023} [I(n) + jQ(n)](n) e^{-j w_d n T_c} \quad + \quad e^{-j w_d (1023) T_c} \sum_{n=1}^{1023} [I(n+1023) + jQ(n+1023)](n) e^{-j w_d n T_c}$$

$$= S_1 \quad + \quad e^{-j w_d (1023) T_c} S_2$$

Here, S_1 is the first 1ms integration sum and S_2 is the second 1ms integration sum computed using the same rotated C/A values that were used to compute S_1. The term $e^{-jwd(1023)Tc}$ is the phase offset that compensates for using the same rotated values. Similarly, a 3ms coherent integration sum can be expressed as

$$S(3ms) \quad = \quad S_1 \quad + \quad e^{-j w_d (1023) T_c} S_2 \quad + \quad e^{-j w_d (2046) T_c} S_3$$

So to extend the integration time while using the same 1023-element rotated C/A sequence, the (n+1) 1ms integration sum should be multiplied by $e^{-jwdn(1ms)}$ before being added to the whole sum. Since this is a rotation of 1ms integration sums, we can combine this operation with the frequency search to avoid having to perform 2 rotations. That is, since

$$e^{-j w_d n(1ms)} e^{-j w_n n(1ms)} \quad = \quad e^{-j(w_d + w_n) n(1ms)}$$

we can multiply the (n+1)th 1ms integration sum by $e^{j(wd+wh)n(1ms)}$ to search a frequency hypothesis and account for the frequency Doppler phase offset.

Note that the frequency search can be reduced after acquiring one satellite, because the frequency uncertainty is not dependent on the satellite. A much finer frequency search can be performed if a longer coherent integration is desired.

In the exemplary embodiment of the invention, the fine search is performed in similar manner the coarse search with 2 differences. First, the integration intervals are always added coherently instead of squaring and adding noncoherently. Second, the rotation to remove the frequency uncertainty (which should be known after the coarse search) is combined with the frequency Doppler phase offset and used to rotate the 1ms coherent integration intervals before adding them together.

In an alternative embodiment of the invention, the coherent integration window of chipx2 data is integrated for integration times longer than 18ms. This embodiment is useful were additional memory is available. For coherent integrations longer than 18ms, the 50Hz data boundaries are treated the same as with shorter integration periods. The base station indicates where the boundaries are for each satellite and the DSP

decides whether to add or subtract the sum of 20 1ms coherent integration intervals to or from its running sum.

However, because the product of the frequency uncertainty and the integration time constant affects the loss in Ec/Nt, the frequency uncertainty must be reduced to very small levels for long coherent integration intervals. Since a 20ms integration with a 20Hz frequency uncertainty resulted in a loss in Ec/Nt of 2.42 dB, maintaining the same loss with an integration time of 400ms requires that the frequency uncertainty be reduced to 1Hz. To correct for this problem, the frequency uncertainty is reduced down to 1Hz in a hierarchical manner. For example, a first frequency search reduces the uncertainty from 100Hz to 20Hz, a second search reduces the uncertainty to 4 Hz, and a third search reduces the uncertainty to 1Hz. The frequency search will also compensate for errors in the frequency Doppler obtained from the base station.

Additionally, to perform longer integrations only satellites with similar Doppler are searched over the same data for long integration times, since the code Doppler is different for each satellite. The DSP computes how long it takes to slip 1/16 of a chip and slews the decimator as it collects a coherent integration data window. Additionally, multiple data windows are taken in this embodiment.

Thus, a method and apparatus for performing position location in wireless communications system has been described. The previous description of the preferred embodiments is provided to enable any person skilled in the art to make or use the present invention. The various modifications to these embodiments will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other embodiments without the use of the inventive faculty. Thus, the present invention is not intended to be limited to the embodiments shown herein but is to be accorded the widest scope consistent with the principles and novel features disclosed herein.

WHAT IS CLAIMED IS:

CLAIMS

1. A method for performing position location using a set of signals transmitted from a set of satellites comprising the steps of:

(a) storing coarse search data;

(b) performing a coarse search on said coarse search data for each satellite from said set of satellites;

(c) receiving fine search data;

(d) performing a set of fine searches on said fine search data, each fine search being performed on a different time segment of said fine search data;

(e) reporting results.

2. The method as set forth in claim 1 wherein said coarse search is performed over at lower resolution, and said fine search is performed at higher resolution.

3. The method as set forth in claim 2 wherein said fine search is performed over a window centered at offset corresponding to said coarse search results.

4. The method as set forth in claim 1 wherein said each fine search and each coarse search are performed over a duration of samples that corresponds to more than a 10 ms duration.

5. The method as set forth in claim 4 wherein each coarse search is performed over a substantially identical portion of said coarse search data.

6. The method as set forth in claim 1 further wherein said fine search data is deleted after processing, but before said fine search has been completed.

7. The method as set forth in claim 1 wherein said fine searches are performed for each of said satellites.

8. The method of claim 2 wherein said lower resolution is chipx4 or lower and said higher resolution is chipx8 or higher.

9. The method of claim 2 wherein said lower resolution is chipx2 or lower and said higher resolution is chipx4 or higher.

10. The method as set forth in claim 1 wherein said different time segments overlap.

11. A method for performing position location in a wireless communication system using a set of signals transmitted from a set of satellites comprising the steps of:

(a) collecting approximately 18ms of lower resolution samples;

(b) performing a set of coarse searches over said lower resolution samples;

(c) computing acquisition codes based on said set of coarse search;

(d) start collecting higher resolution samples;

(e) performing a set of fine searches on said higher resolution samples;

(f) ending collection of higher resolution samples.

12. The method as set forth in claim 11 wherein step (e) is comprised of the repeatedly performed steps of:

(e.1) adjusting a phase of a sampling clock;

(e.2) performing a fine search for a signal from one satellite.

13. The method as set forth in claim 11 wherein said lower resolution samples are chipx2 samples.

14. The method as set forth in claim 11 wherein said higher resolution samples are chipx8 samples.

15. The method as set forth in claim 11 further comprising the step of transmitting reverse link frames to said base station.

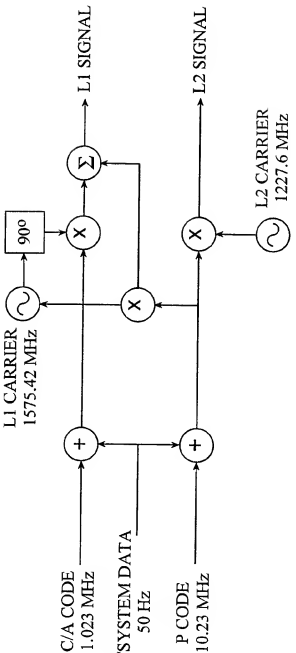

C/A CODE
1.023 MHz
NAV/SYSTEM DATA
50 Hz
P CODE
10.23 MHz
L1 CARRIER
1575.42 MHz
90°
L2 CARRIER
1227.6 MHz
L1 SIGNAL
L2 SIGNAL

FIG. 1

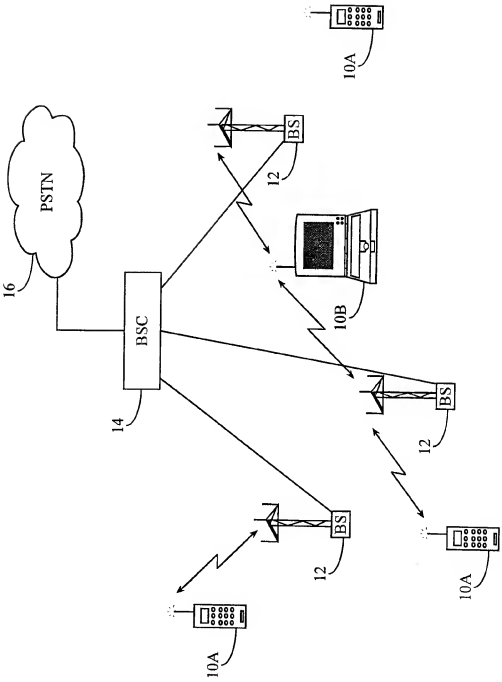


FIG. 2

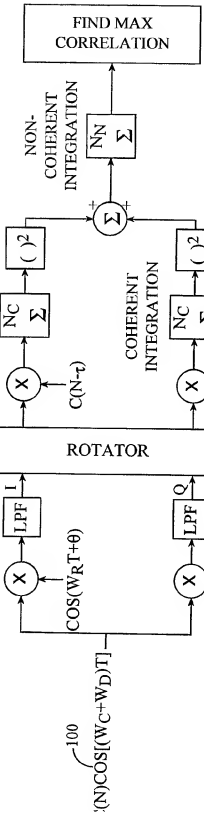

FIND MAX CORRELATION
NON-COHERENT INTEGRATION
N_N Σ
Σ
( )²
( )²
104
N_C Σ
N_C Σ
104
COHERENT INTEGRATION
C(N-τ)
C(N-τ)
102
ROTATOR
LPF
I
LPF
Q
COS(W_RT+θ)
SIN(W_RT+θ)
100
:(N)COS[(W_C-W_D)T]

FIG. 3

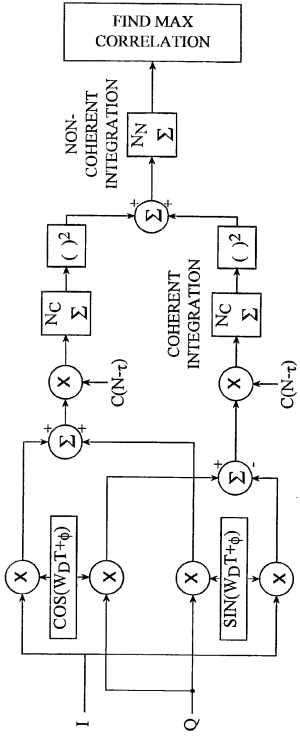

FIND MAX CORRELATION
NON-COHERENT INTEGRATION
N_N Σ
( )2
( )2
N_C Σ
N_C Σ
COHERENT INTEGRATION
C(N-τ)
C(N-τ)
COS(W_DT+φ)
SIN(W_DT+φ)
I
Q

FIG. 4

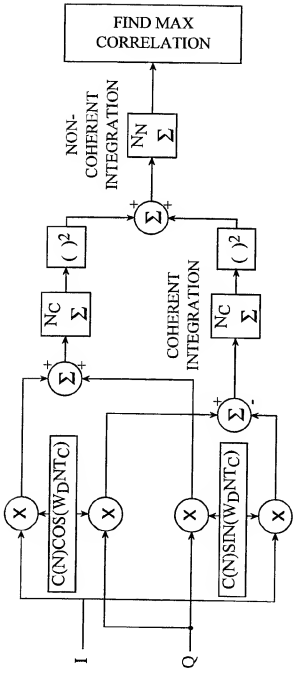
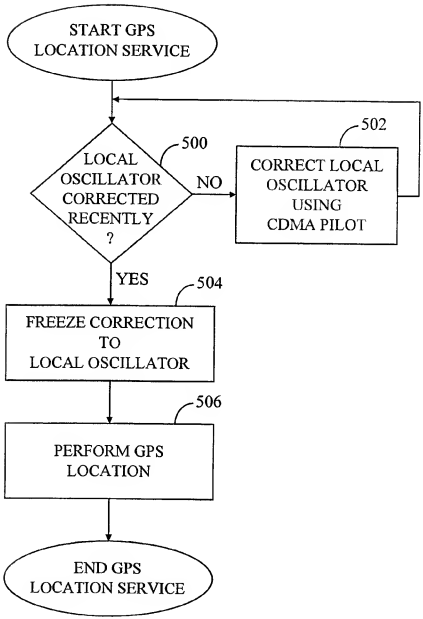

FIND MAX CORRELATION
NON-COHERENT INTEGRATION
NN Σ
( )2
( )2
Σ
Nc Σ
Nc Σ
COHERENT INTEGRATION
C(N)COS(WDNTc)
C(N)SIN(WDNTc)
I
Q

FIG. 5


START GPS LOCATION SERVICE
LOCAL OSCILLATOR CORRECTED RECENTLY ?
500
NO
CORRECT LOCAL OSCILLATOR USING CDMA PILOT
502
YES
FREEZE CORRECTION TO LOCAL OSCILLATOR
504
PERFORM GPS LOCATION
506
END GPS LOCATION SERVICE

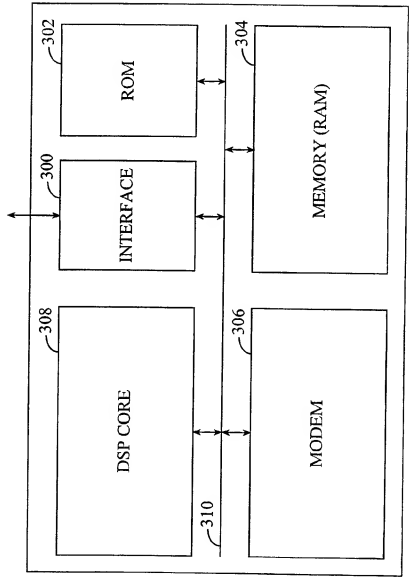
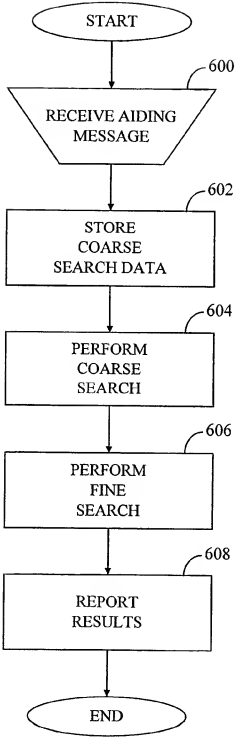

302
ROM
304
MEMORY (RAM)
300
INTERFACE
308
DSP CORE
306
MODEM
310

FIG. 7


START
600
RECEIVE AIDING MESSAGE
602
STORE COARSE SEARCH DATA
604
PERFORM COARSE SEARCH
606
PERFORM FINE SEARCH
608
REPORT RESULTS
END

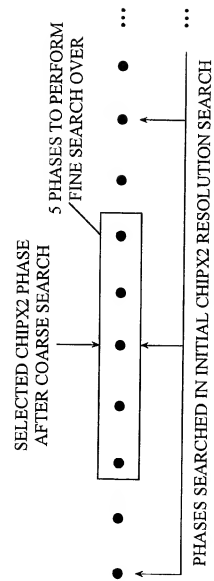

SELECTED CHIPX2 PHASE
AFTER COARSE SEARCH
5 PHASES TO PERFORM
FINE SEARCH OVER
PHASES SEARCHED IN INITIAL CHIPX2 RESOLUTION SEARCH

FIG. 9

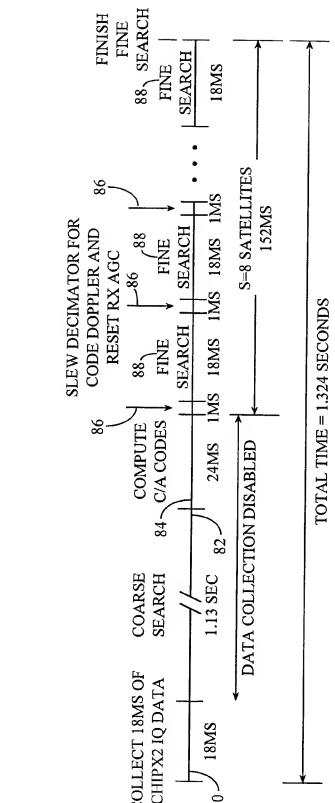

COLLECT 18MS OF CHIPX2 IQ DATA
18MS
80
COARSE SEARCH
1.13 SEC
82
COMPUTE C/A CODES
84
24MS
SLEW DECIMATOR FOR CODE DOPPLER AND RESET RX AGC
86
1MS
FINE SEARCH
88
18MS
1MS
86
FINE SEARCH
88
18MS
1MS
86
FINISH FINE SEARCH
88
18MS
DATA COLLECTION DISABLED
S=8 SATELLITES 152MS
TOTAL TIME = 1.324 SECONDS

FIG. 10

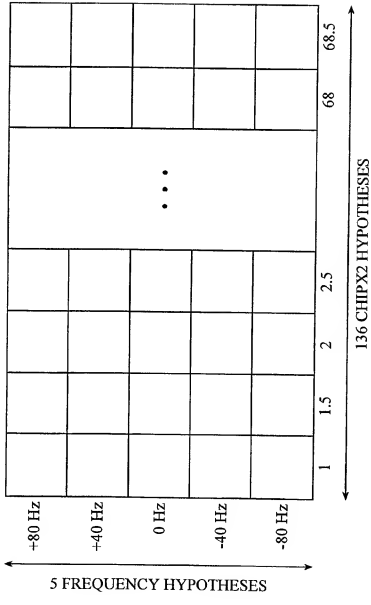

+80 Hz
+40 Hz
0 Hz
-40 Hz
-80 Hz
5 FREQUENCY HYPOTHESES
1
1.5
2
2.5
68
68.5
136 CHIPX2 HYPOTHESES

FIG. 11

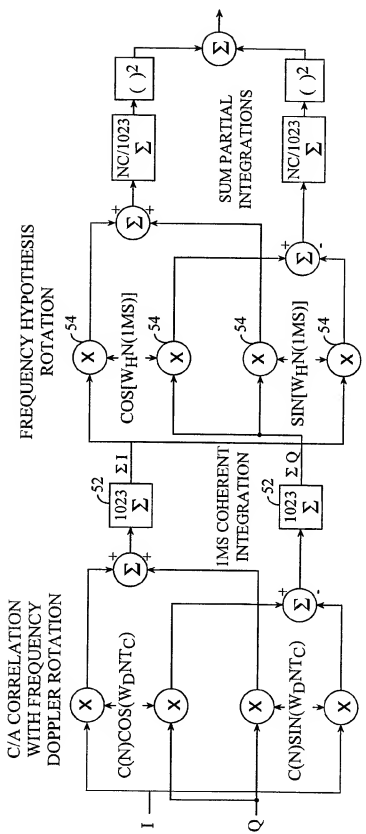

C/A CORRELATION
WITH FREQUENCY
DOPPLER ROTATION
FREQUENCY HYPOTHESIS
ROTATION
1MS COHERENT
INTEGRATION
SUM PARTIAL
INTEGRATIONS
I
Q
C(N)COS(WDNTC)
C(N)SIN(WDNTC)
COS[WHN(1MS)]
SIN[WHN(1MS)]
1023 Σ I
1023 Σ Q
NC/1023 Σ
( )2
52
54

FIG. 12

INTERNATIONAL SEARCH REPORT

Internati Application No
PCT/US 99/20281

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G01S5/14

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G01S

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	HOFMANN-WELLENHOF B. ET AL: "Global Positioning System; Theory and Practice" 1992 , SPRINGER VERLAG , WIEN, AT XP002126677	1-10
Y	page 4, line 6 -page 5, line 18 page 77; table 5.2 page 84, line 14 - line 36	11-15
X	US 5 502 446 A (DENNINGER VALENTINE L) 26 March 1996 (1996-03-26) column 1, line 47 -column 2, line 19	1-10
Y	WO 97 14056 A (SNAPTRACK INC) 17 April 1997 (1997-04-17) page 2, line 14 -page 3, line 23	11-15

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
27 December 1999	24/01/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Haffner, R

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

Internat Application No
PCT/US 99/20281

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5502446 A	26-03-1996	NONE	
WO 9714056 A	17-04-1997	US 5663734 A	02-09-1997
		AU 1131097 A	30-04-1997
		AU 7396096 A	30-04-1997
		AU 7396596 A	30-04-1997
		AU 7397396 A	30-04-1997
		AU 7397596 A	30-04-1997
		AU 7662096 A	30-04-1997
		CA 2230841 A	17-04-1997
		CN 1199468 A	18-11-1998
		CN 1211324 A	17-03-1999
		EP 0880713 A	02-12-1998
		EP 0855041 A	29-07-1998
		EP 0855039 A	29-07-1998
		WO 9714053 A	17-04-1997
		WO 9714054 A	17-04-1997
		WO 9714055 A	17-04-1997
		WO 9714049 A	17-04-1997
		WO 9714057 A	17-04-1997
		US 5831574 A	03-11-1998
		US 5825327 A	20-10-1998
		US 5781156 A	14-07-1998